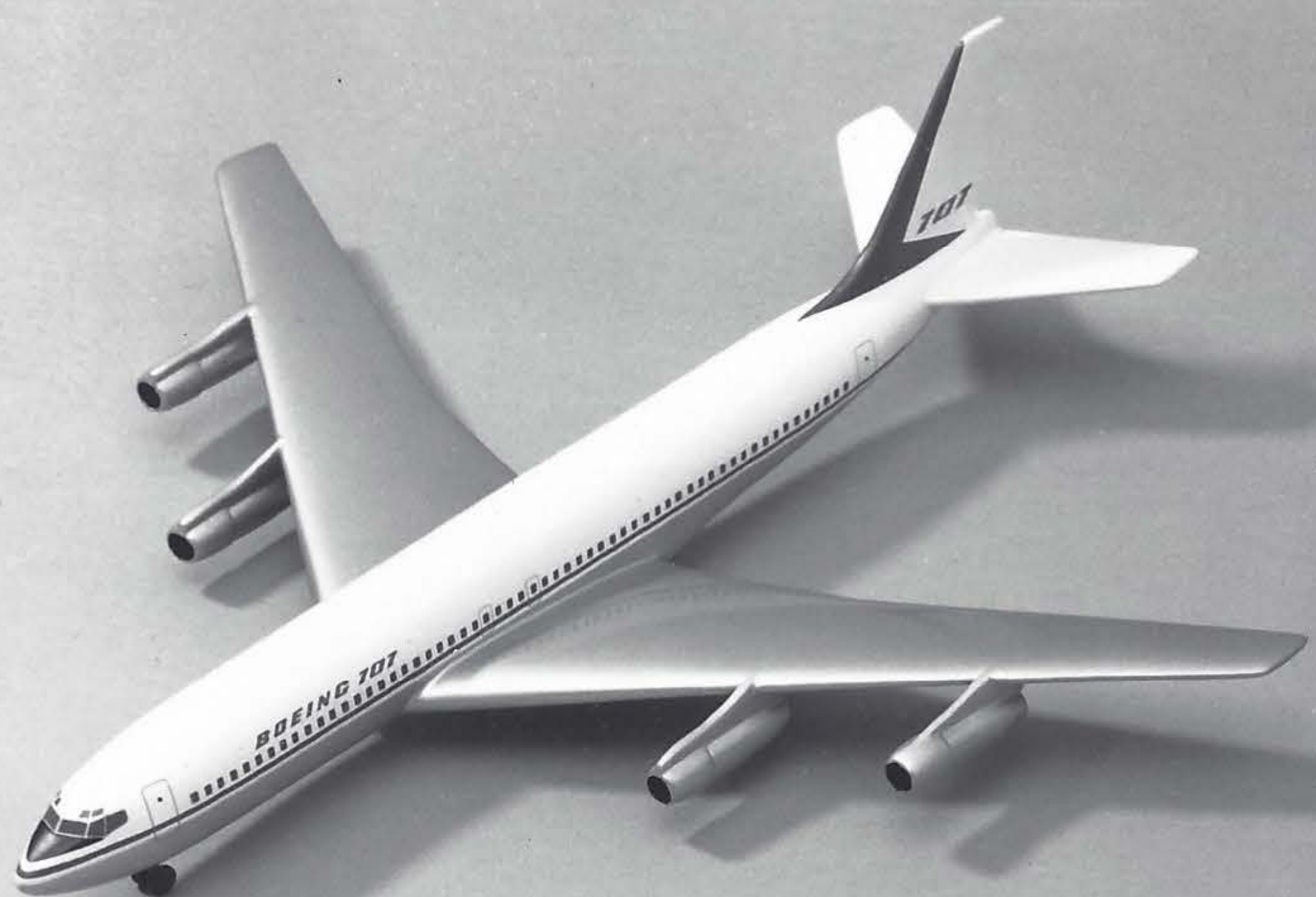
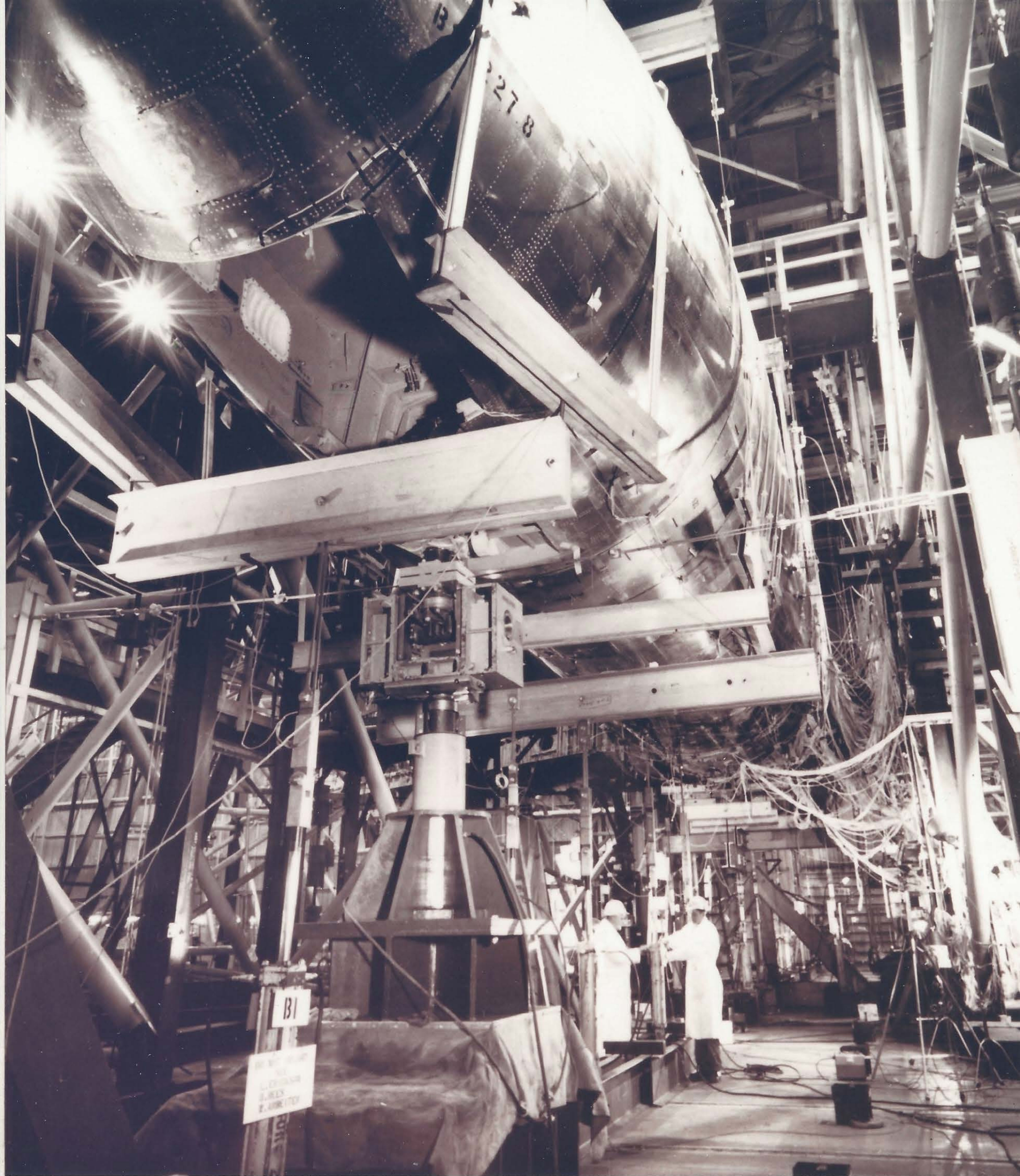


Data System Standardization Study

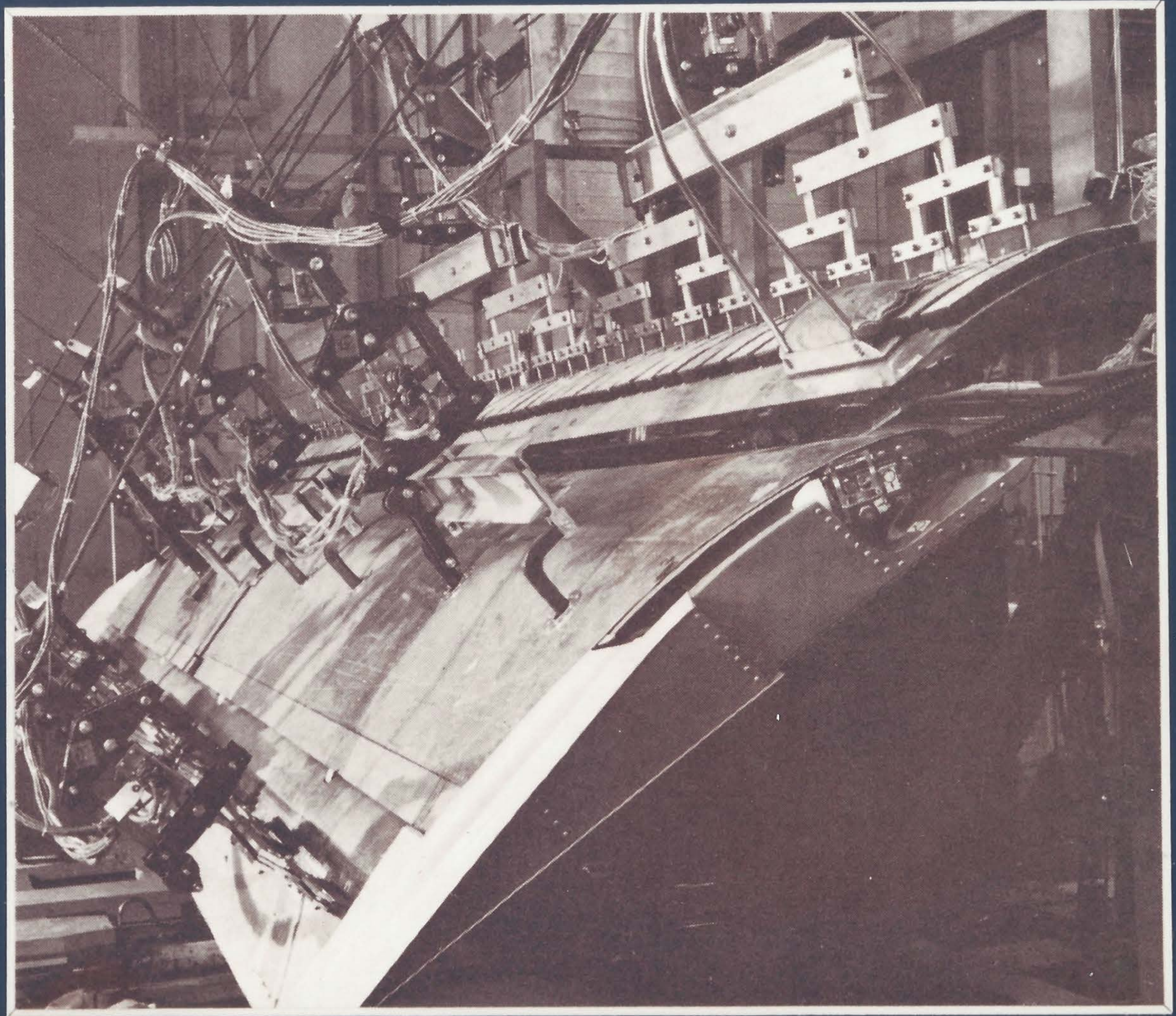
Boeing Engineering Technology Labs



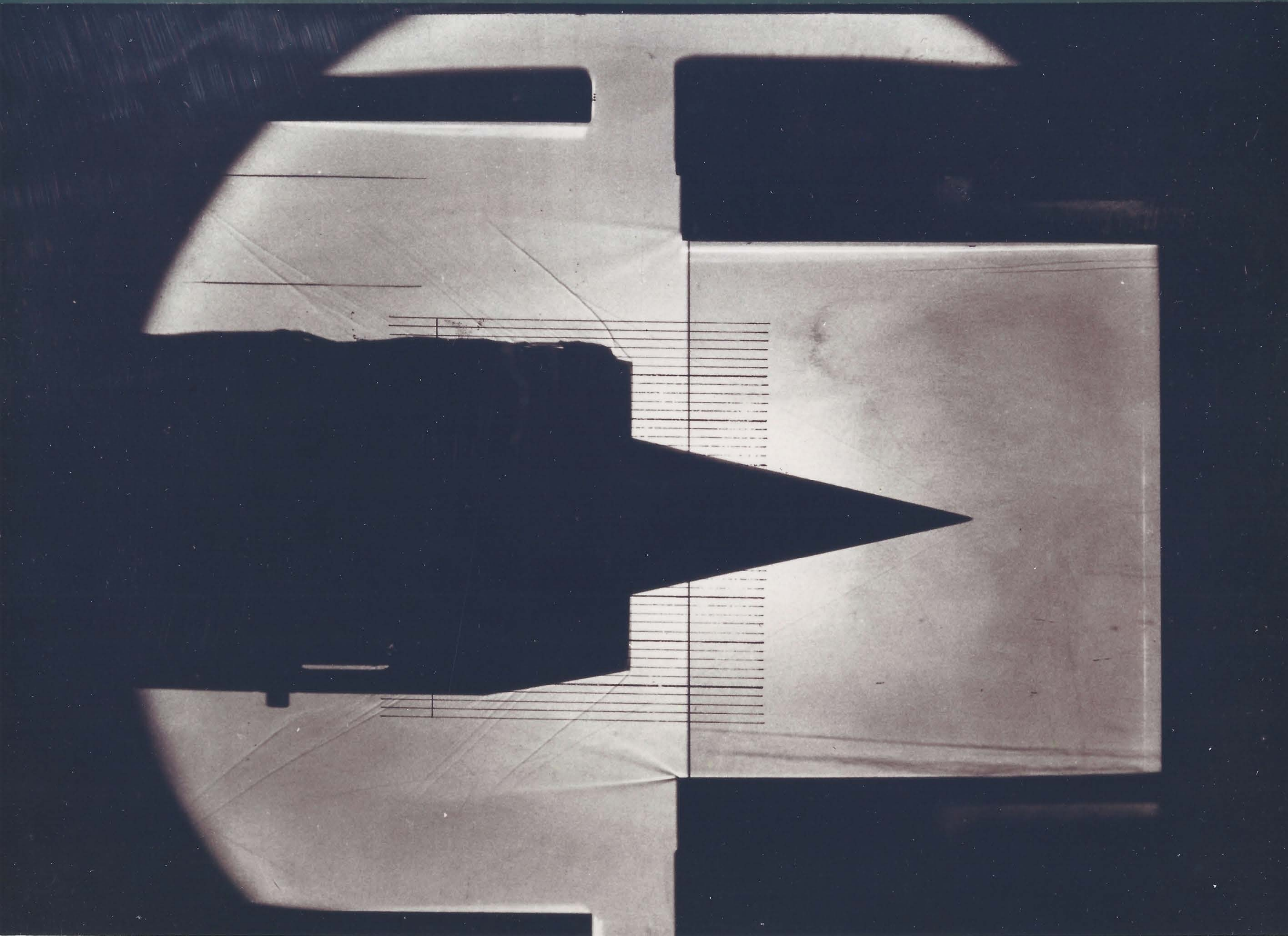
Major Structural Testing



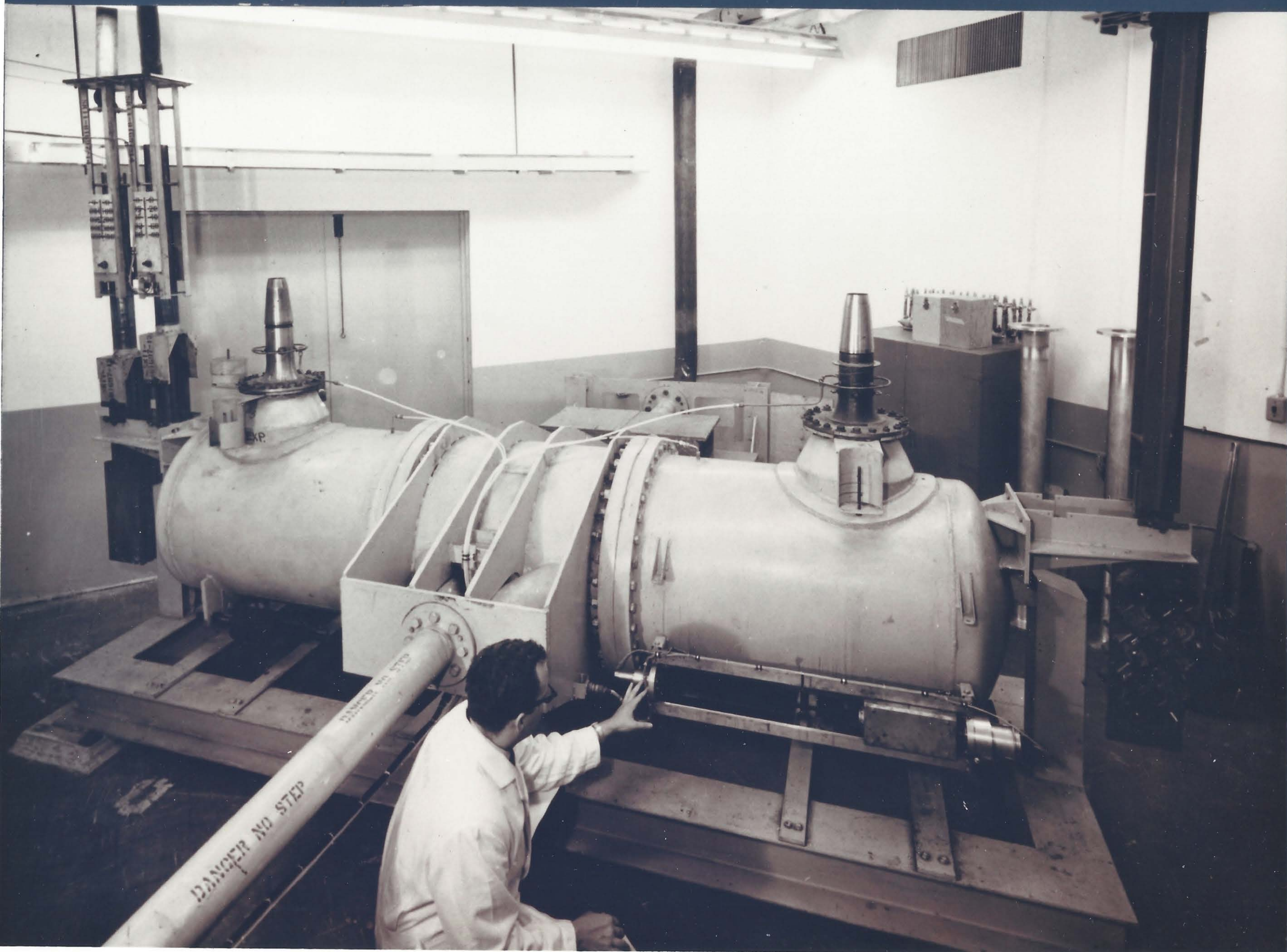
Structural Component Testing



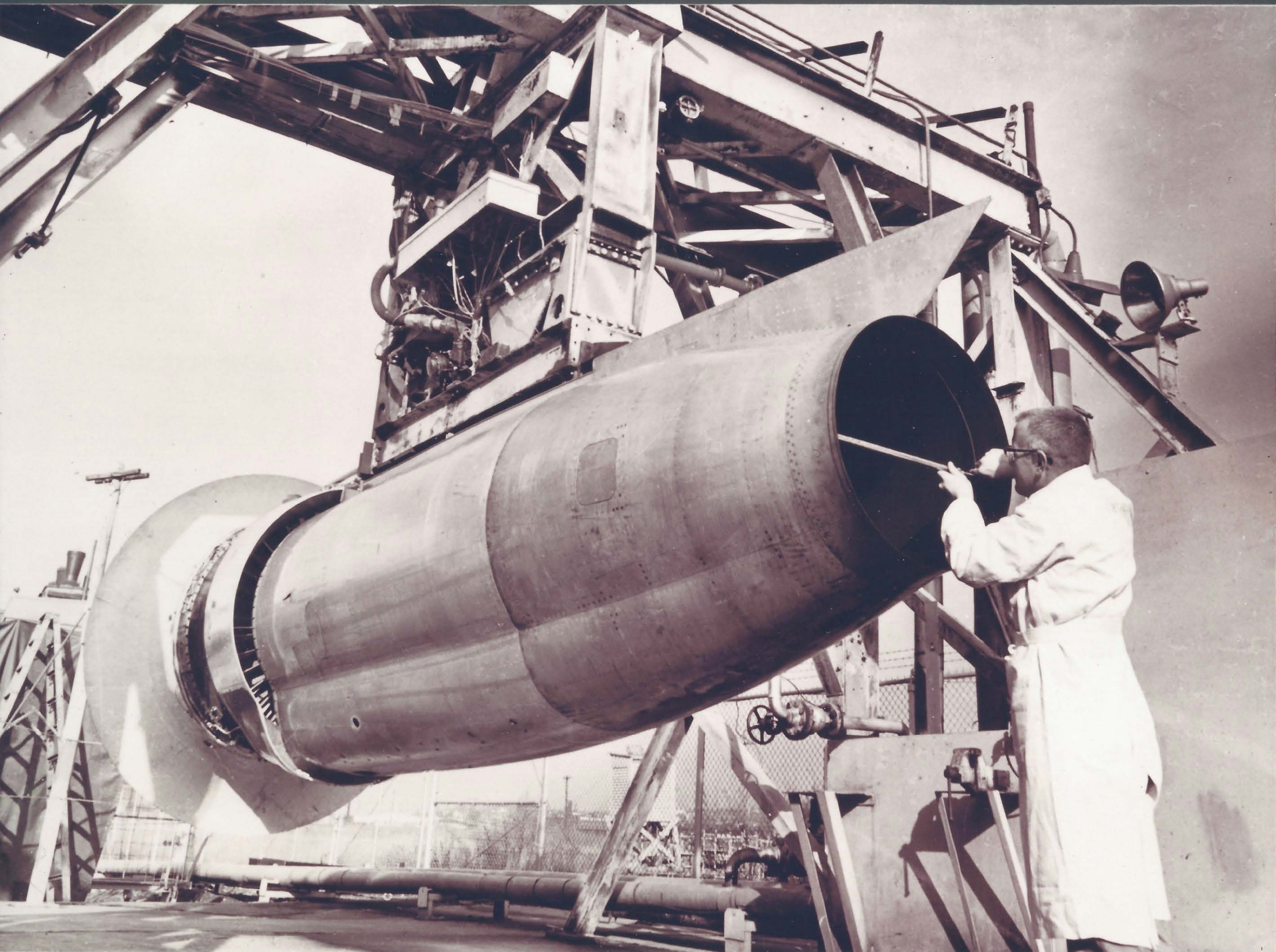
Engine Inlet Testing



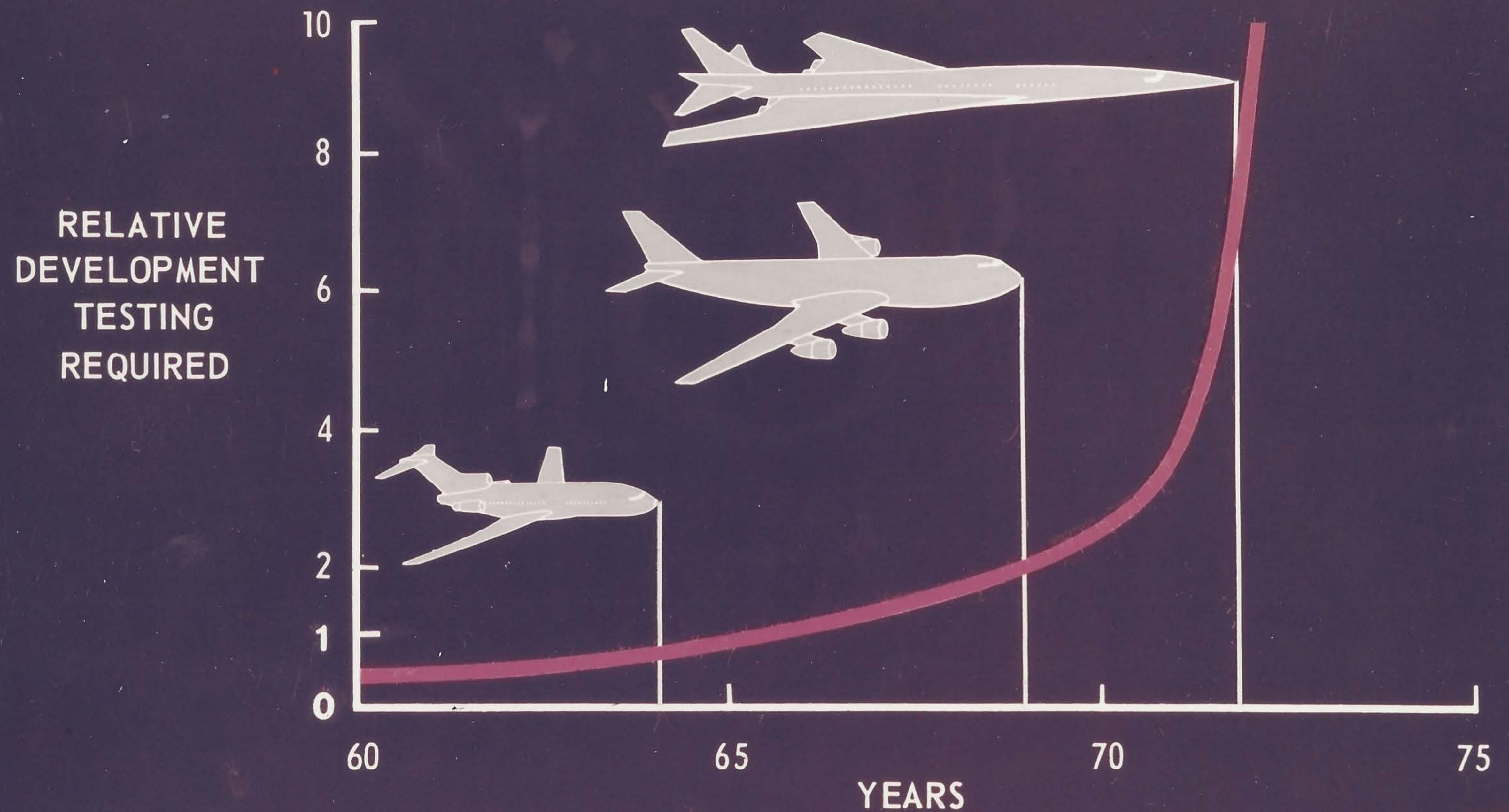
Engine Exhaust Nozzle Testing



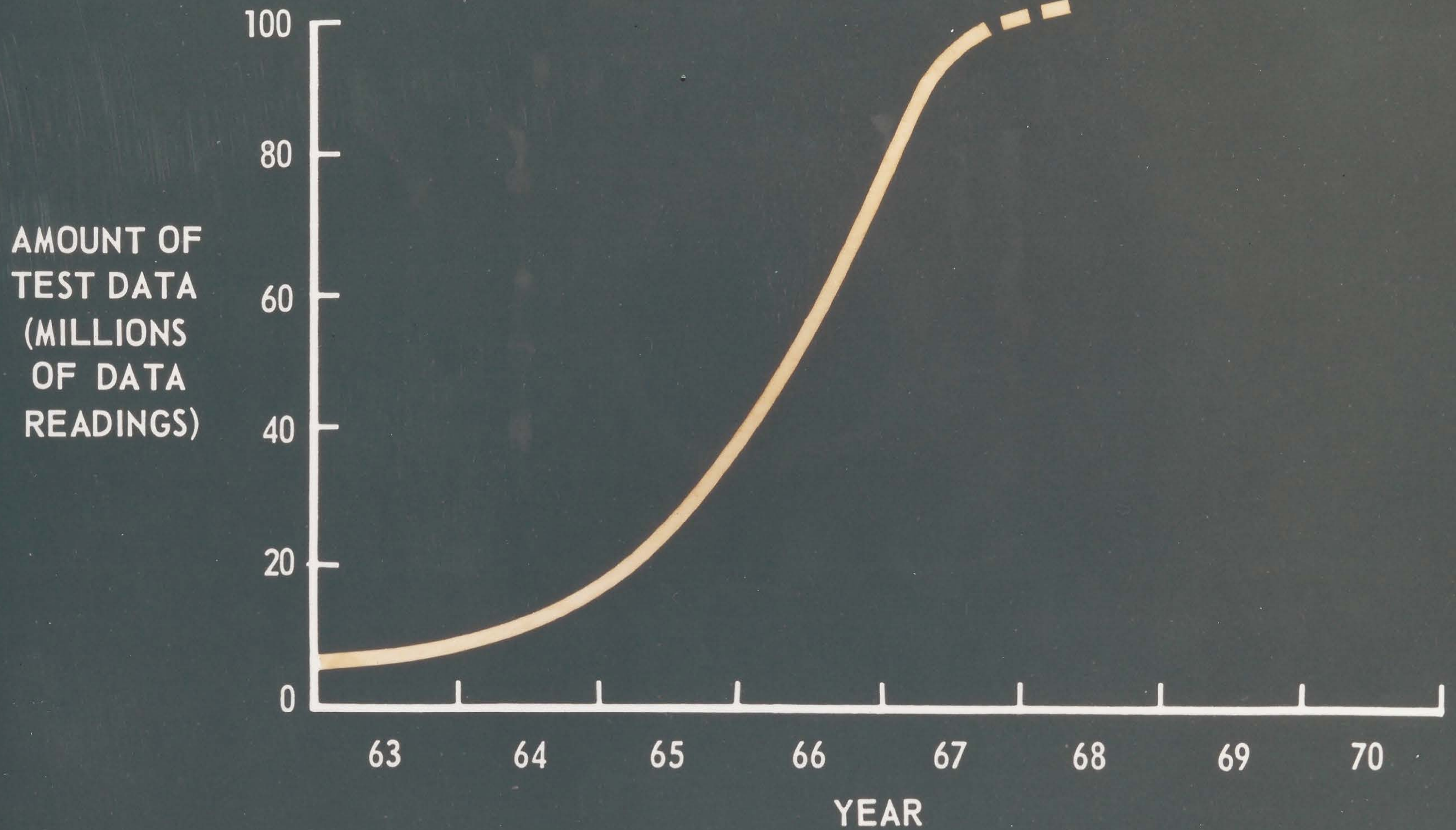
Full-scale Engine Evaluations



Technology Labs Development Testing

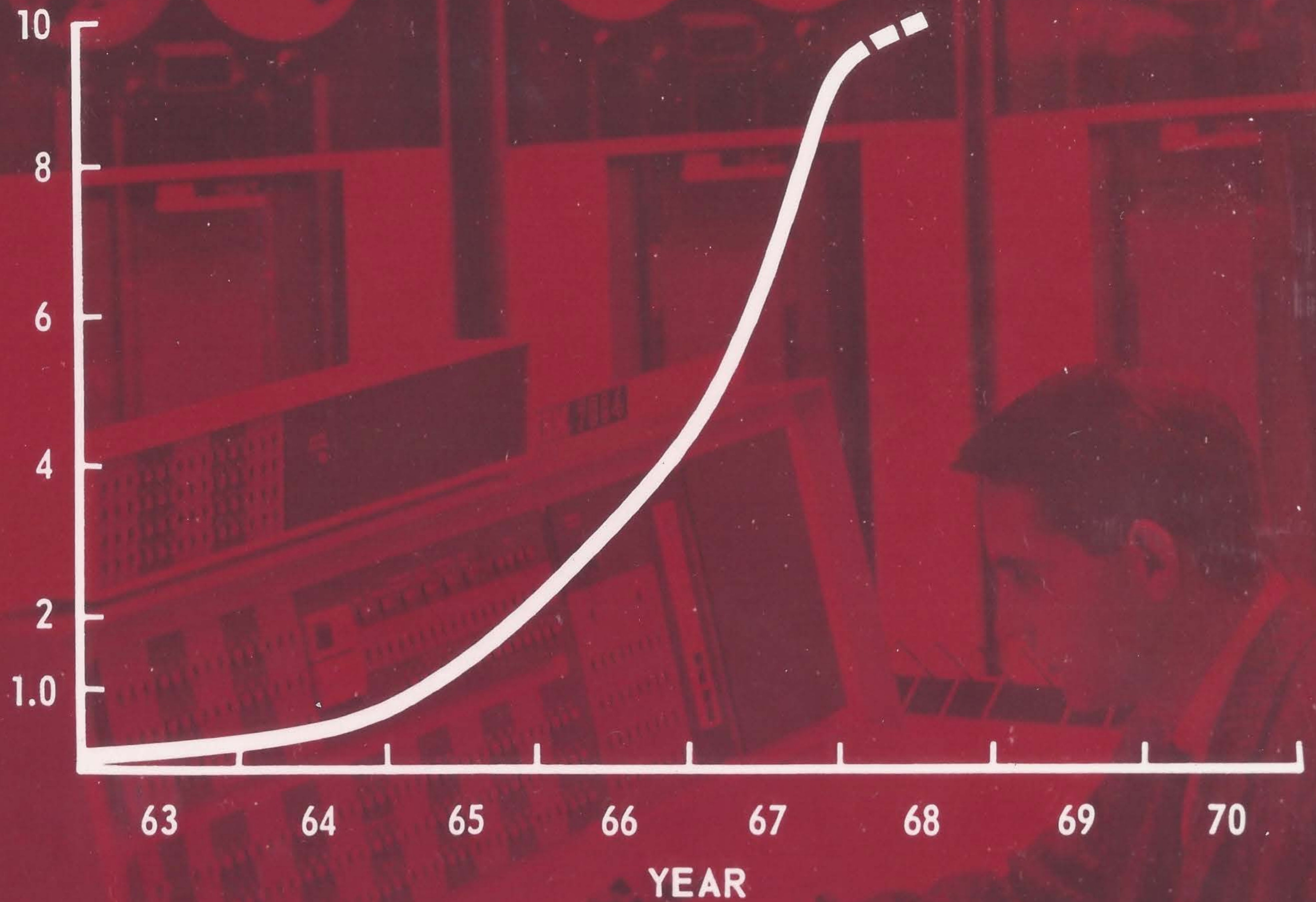


Technology Labs Volume of Test Data

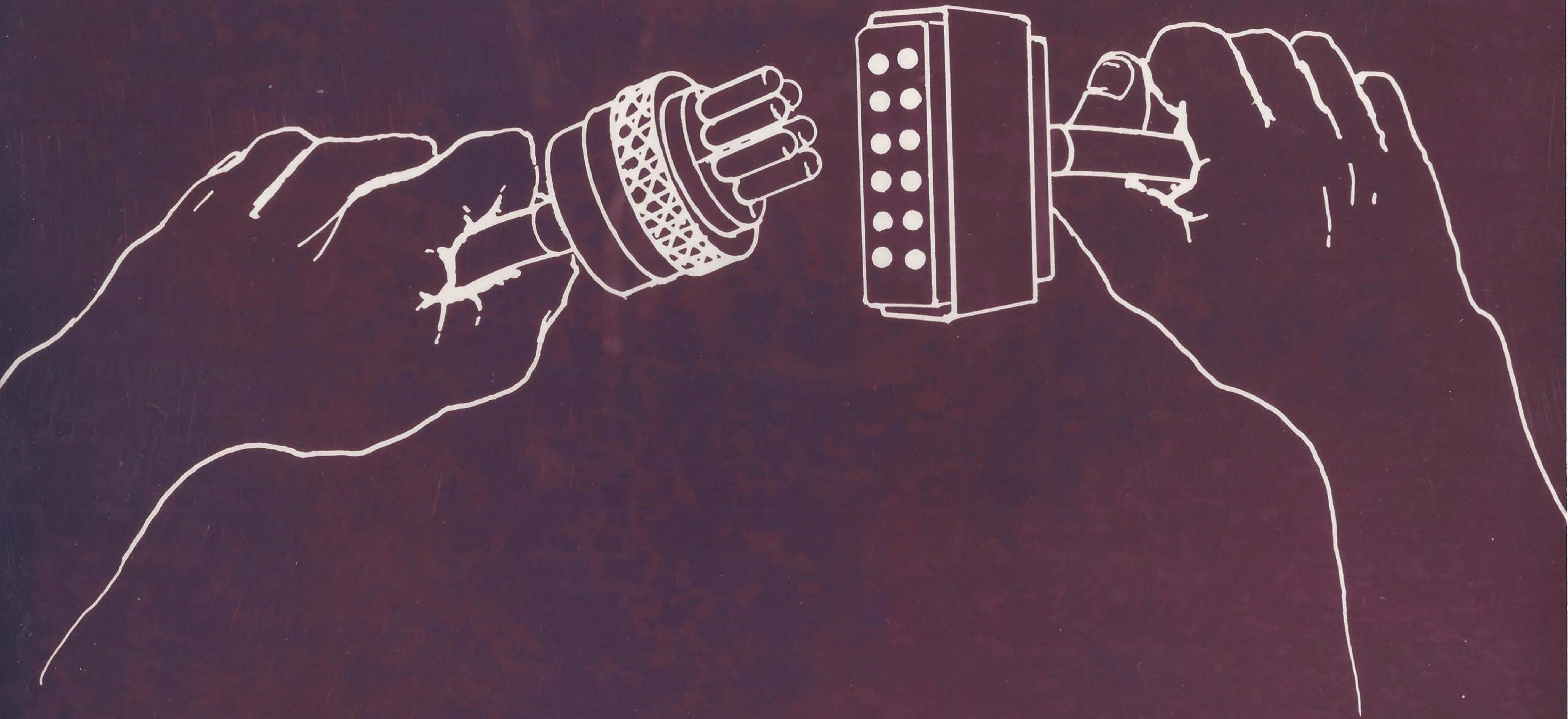


Technology Labs Test Data Processing

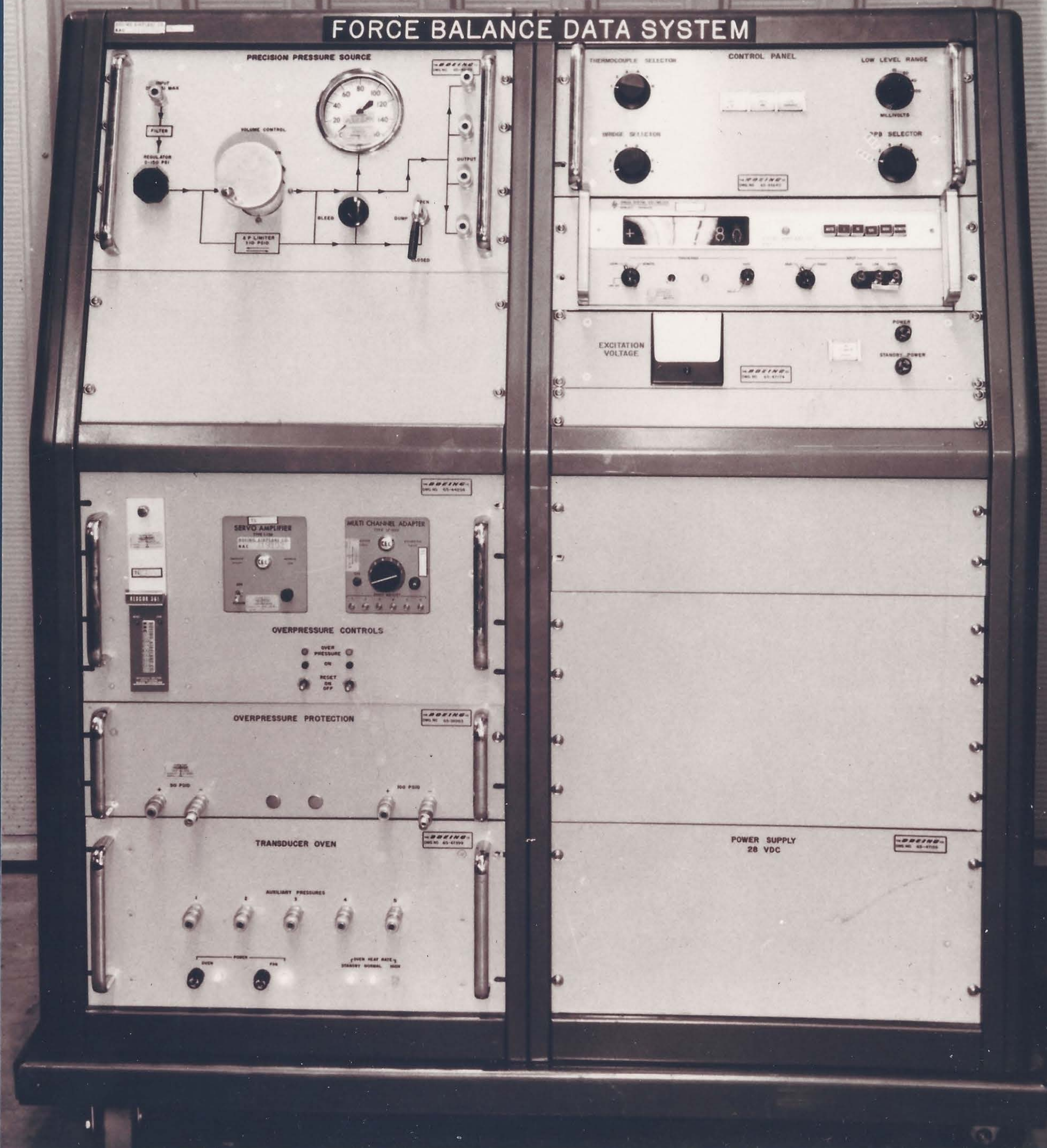
RELATIVE
AMOUNT OF
COMPUTER
SUPPORT



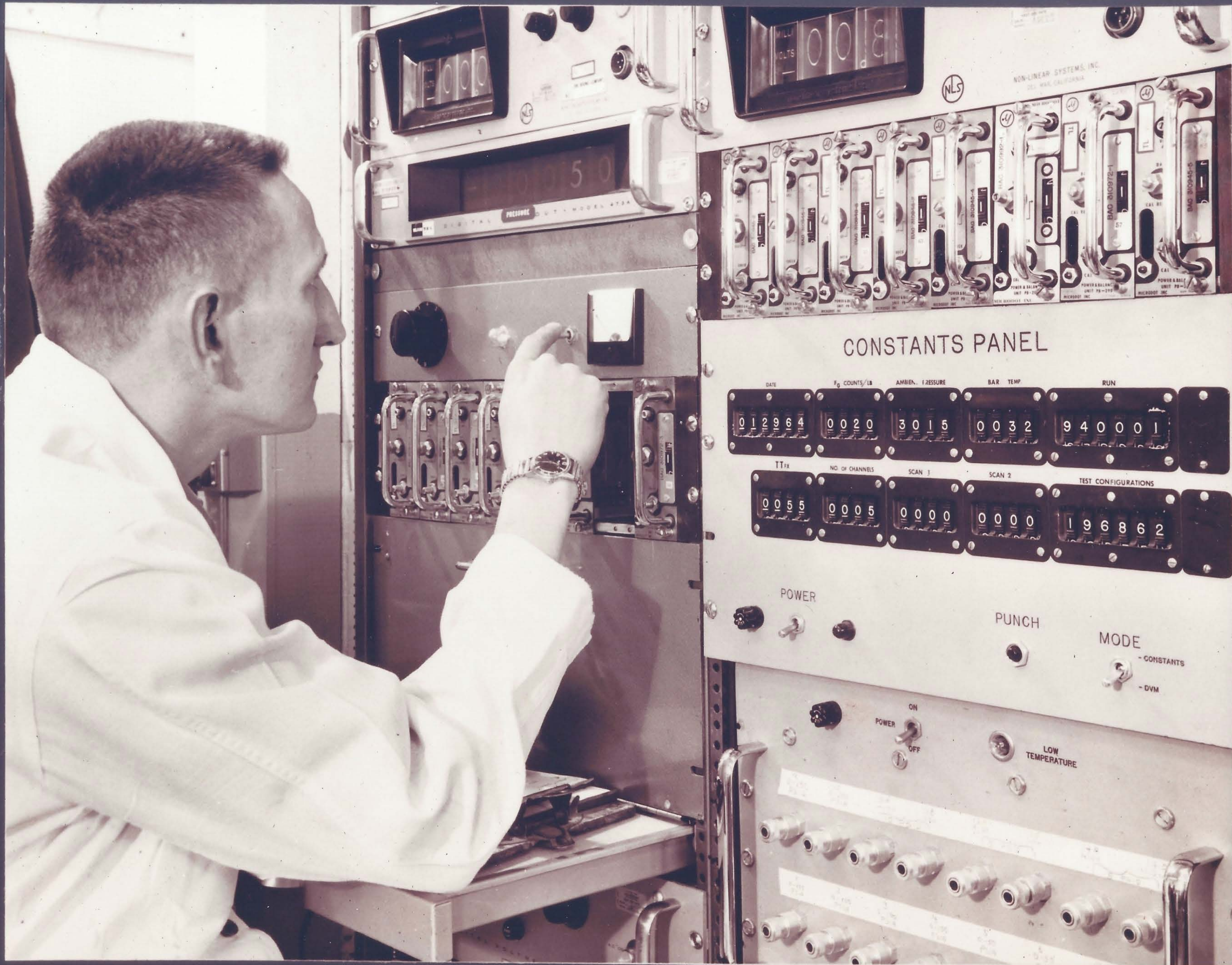
Hardware Incompatability



Present Non-standard Systems





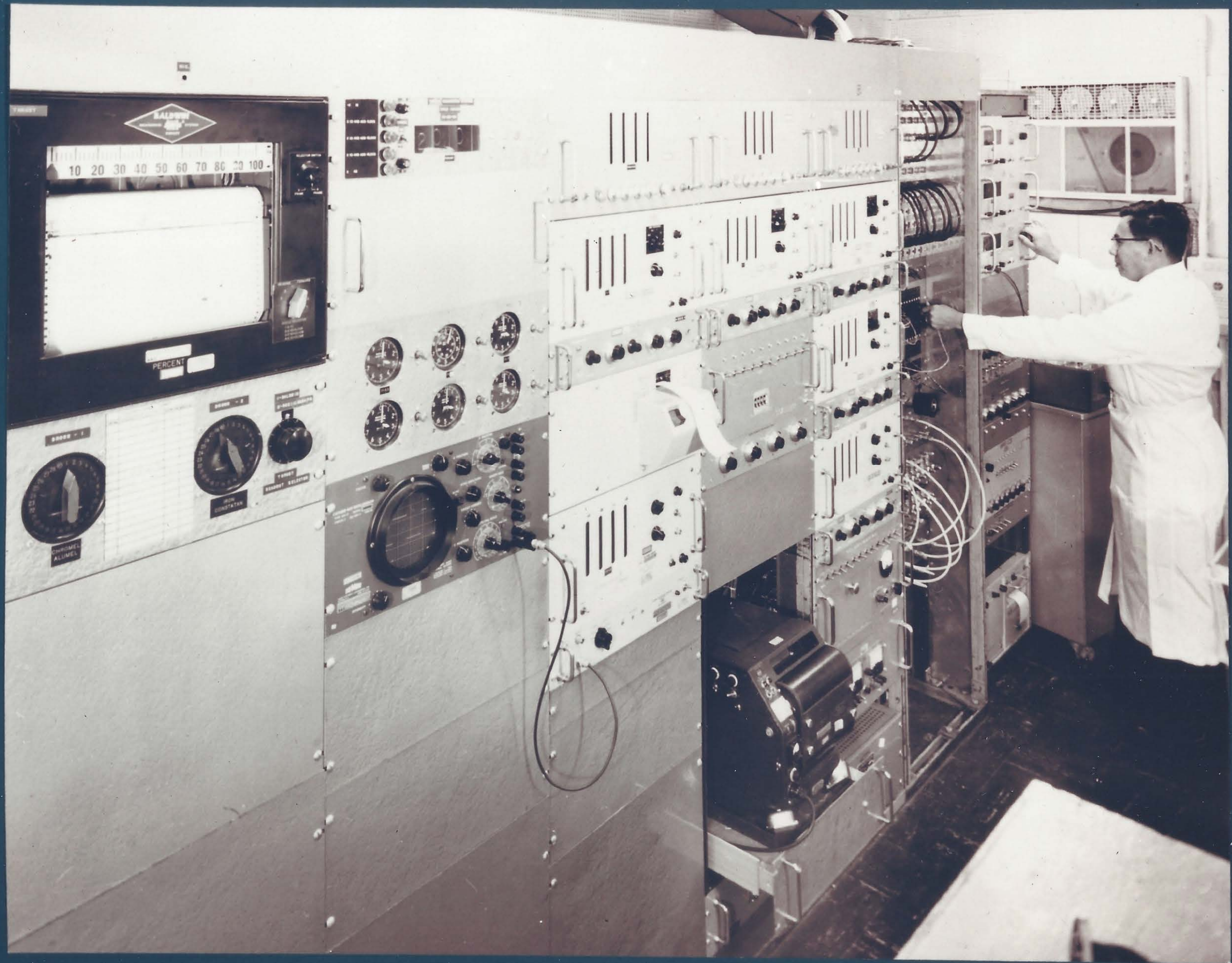


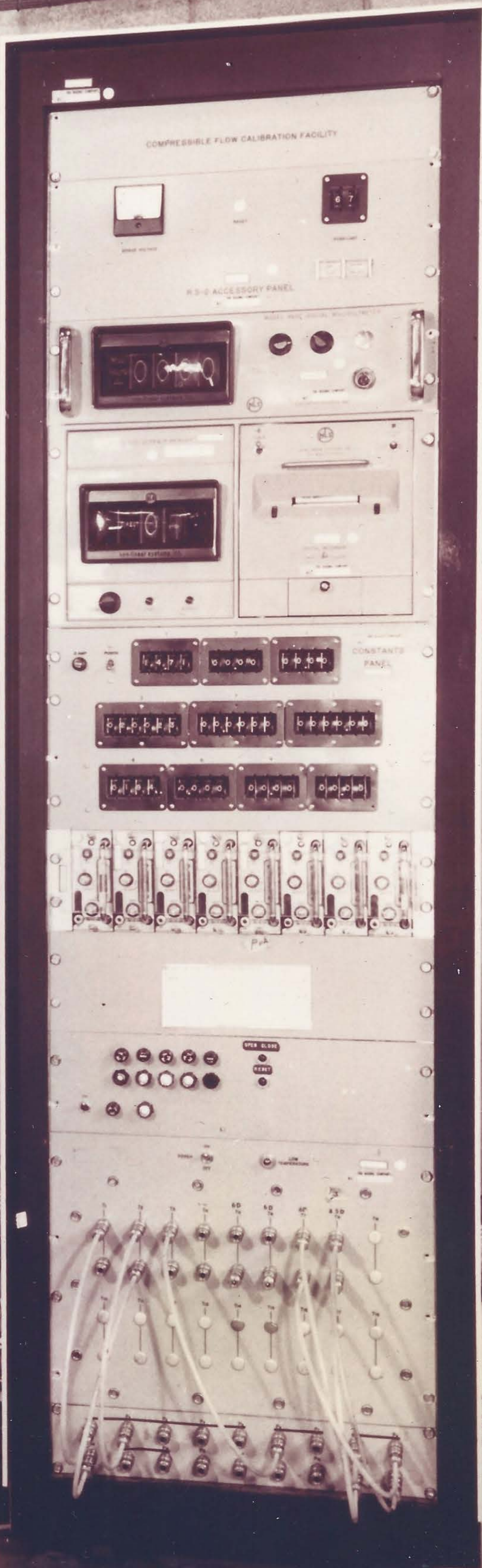
CONSTANTS PANEL

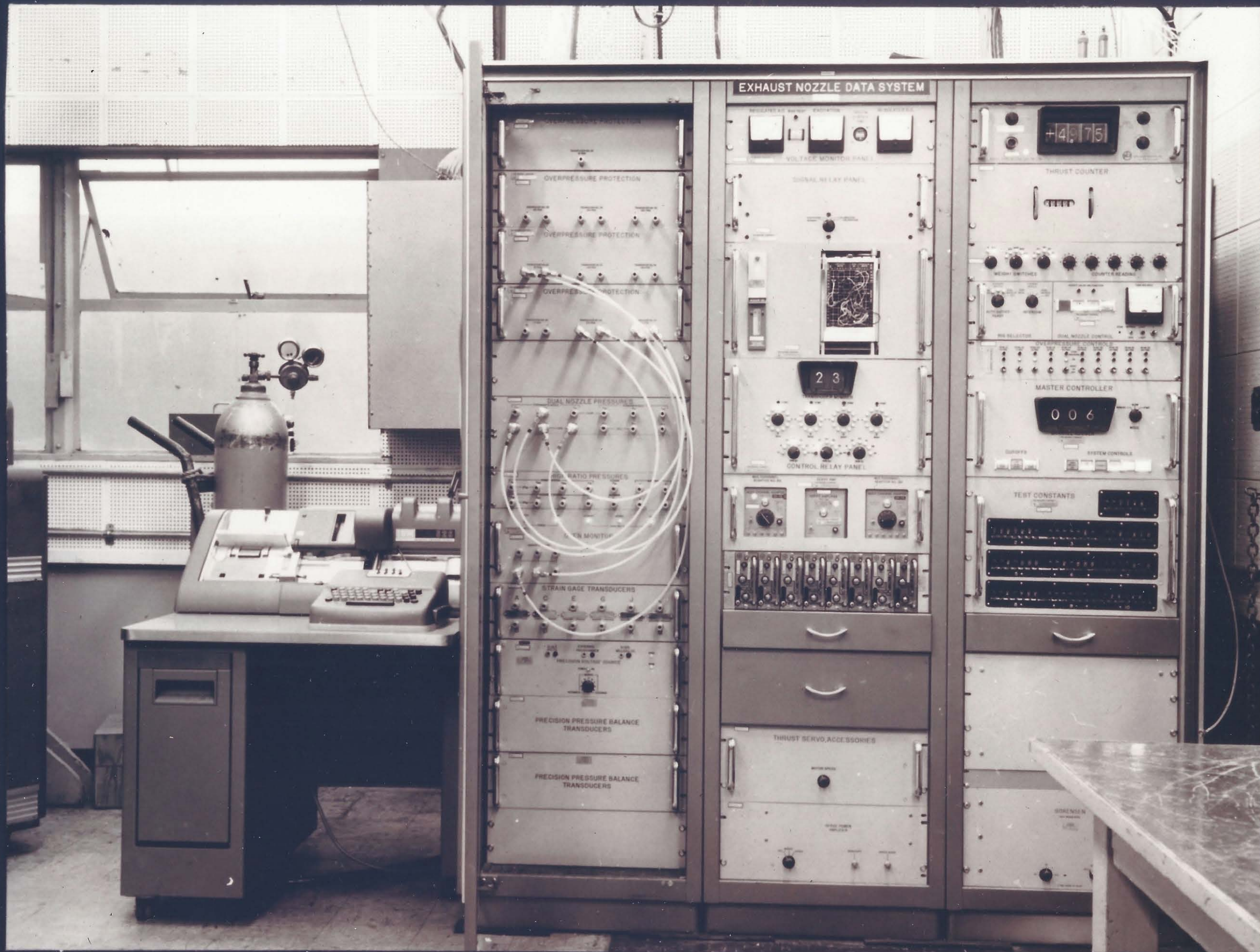
DATE	F ₀ COUNTS/LB	AMBIEN. PRESSURE	BAR TEMP	RUN
012964	0020	3015	0032	940001
TTx	NO OF CHANNELS	SCAN 1	SCAN 2	TEST CONFIGURATIONS
0055	0005	0000	0000	196862

POWER PUNCH MODE
- CONSTANTS
- DVM

ON OFF
POWER LOW TEMPERATURE



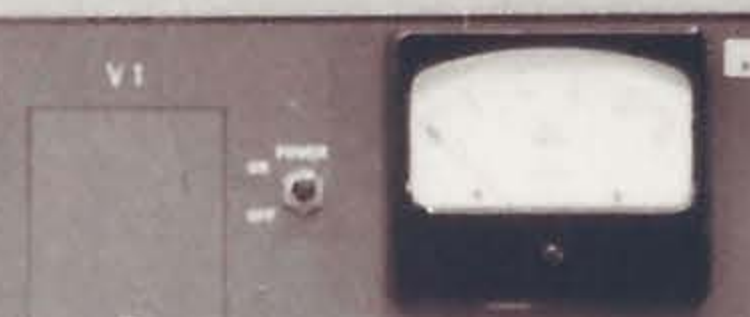
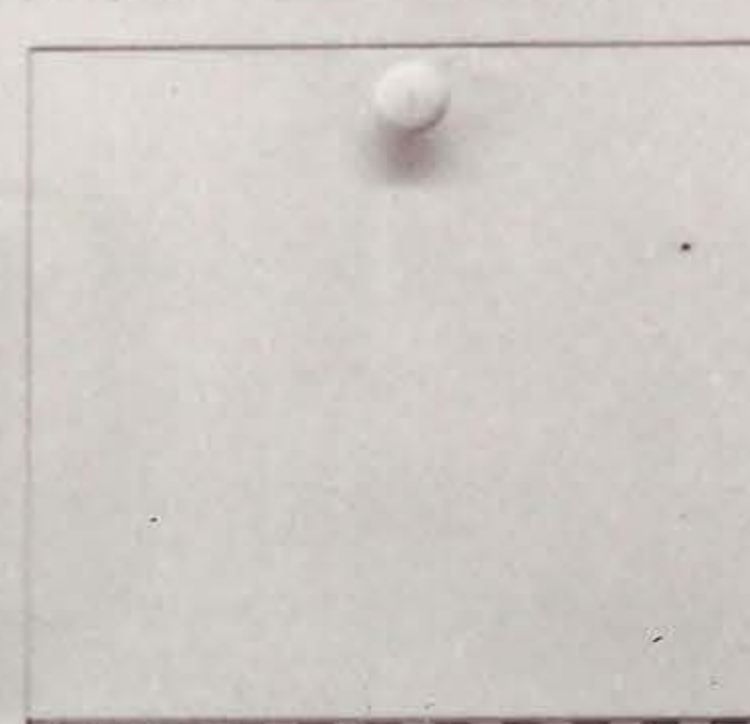
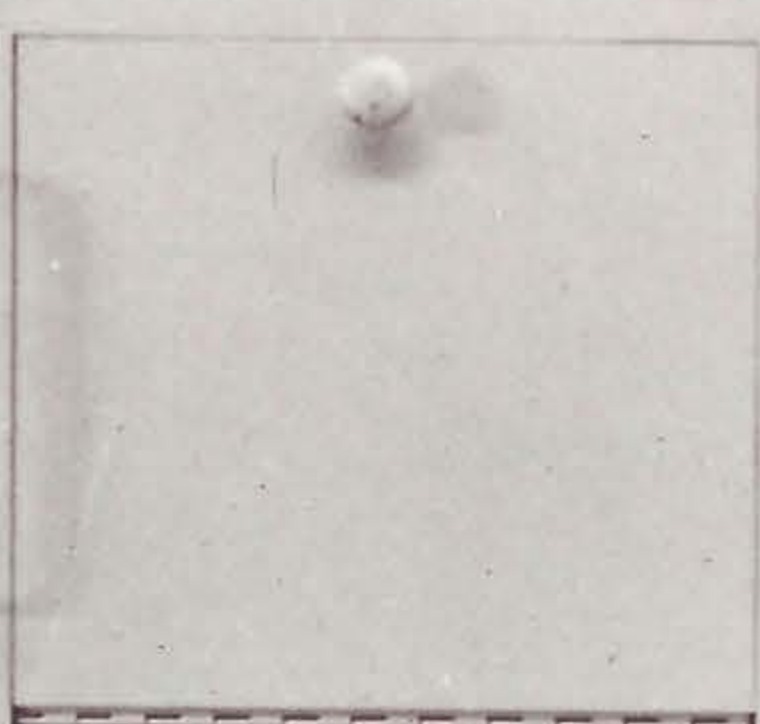
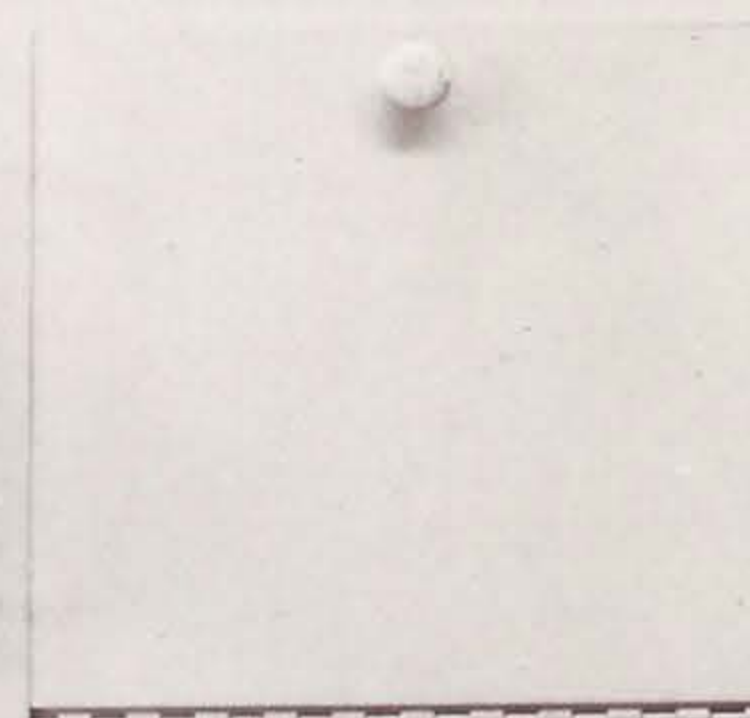




LOAD MONITOR NO. 1

LOAD MONITOR NO. 2

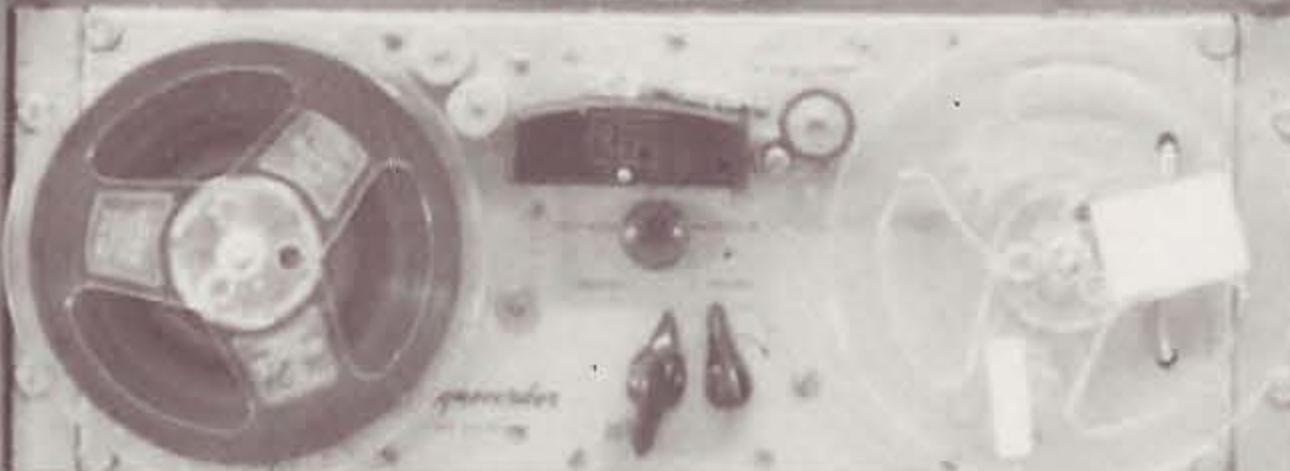
LOAD MONITOR NO. 3



POWER SUPPLY

POWER SUPPLY

POWER SUPPLY

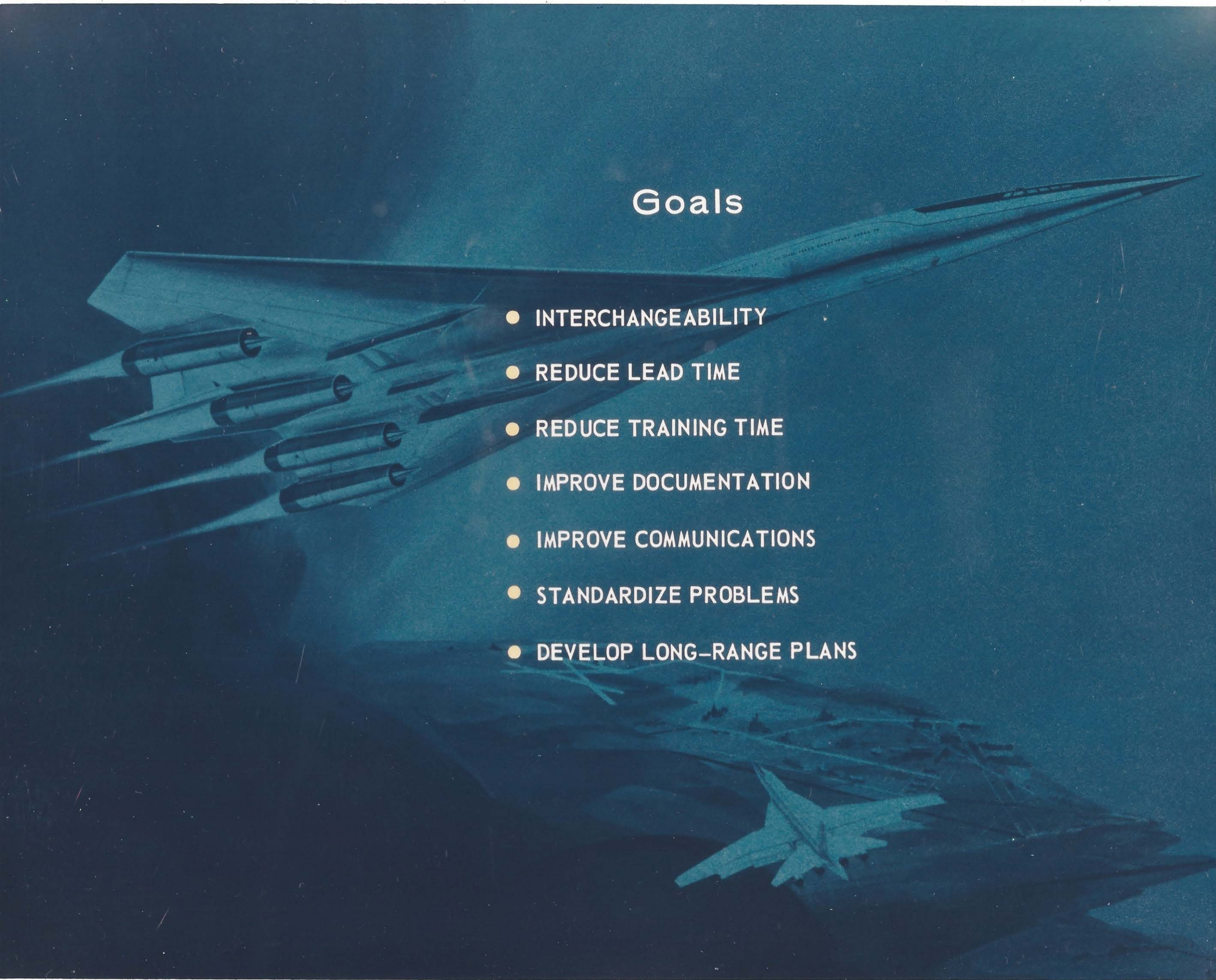






WIND TUNNEL





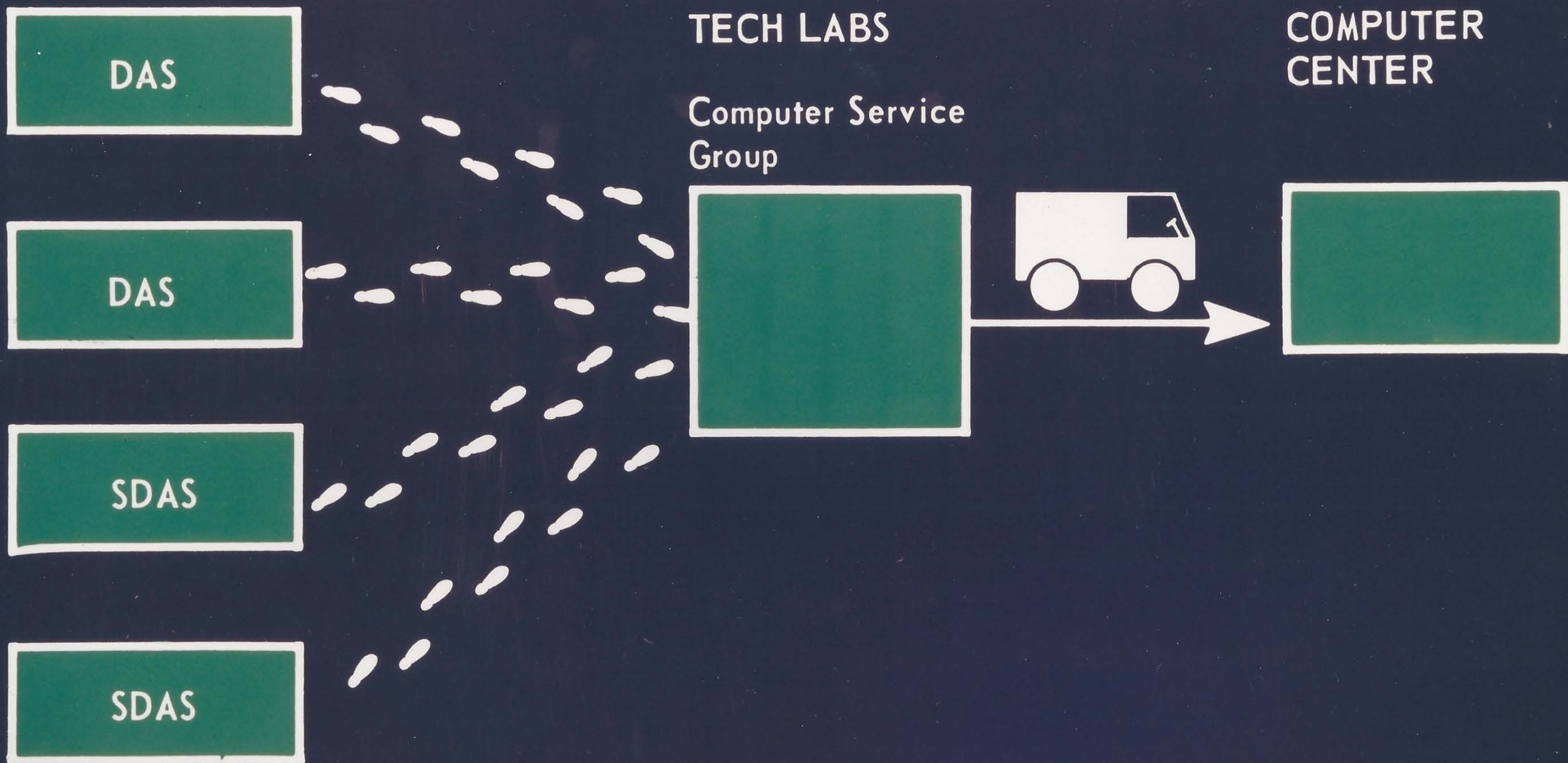
Goals

- INTERCHANGEABILITY
- REDUCE LEAD TIME
- REDUCE TRAINING TIME
- IMPROVE DOCUMENTATION
- IMPROVE COMMUNICATIONS
- STANDARDIZE PROBLEMS
- DEVELOP LONG-RANGE PLANS

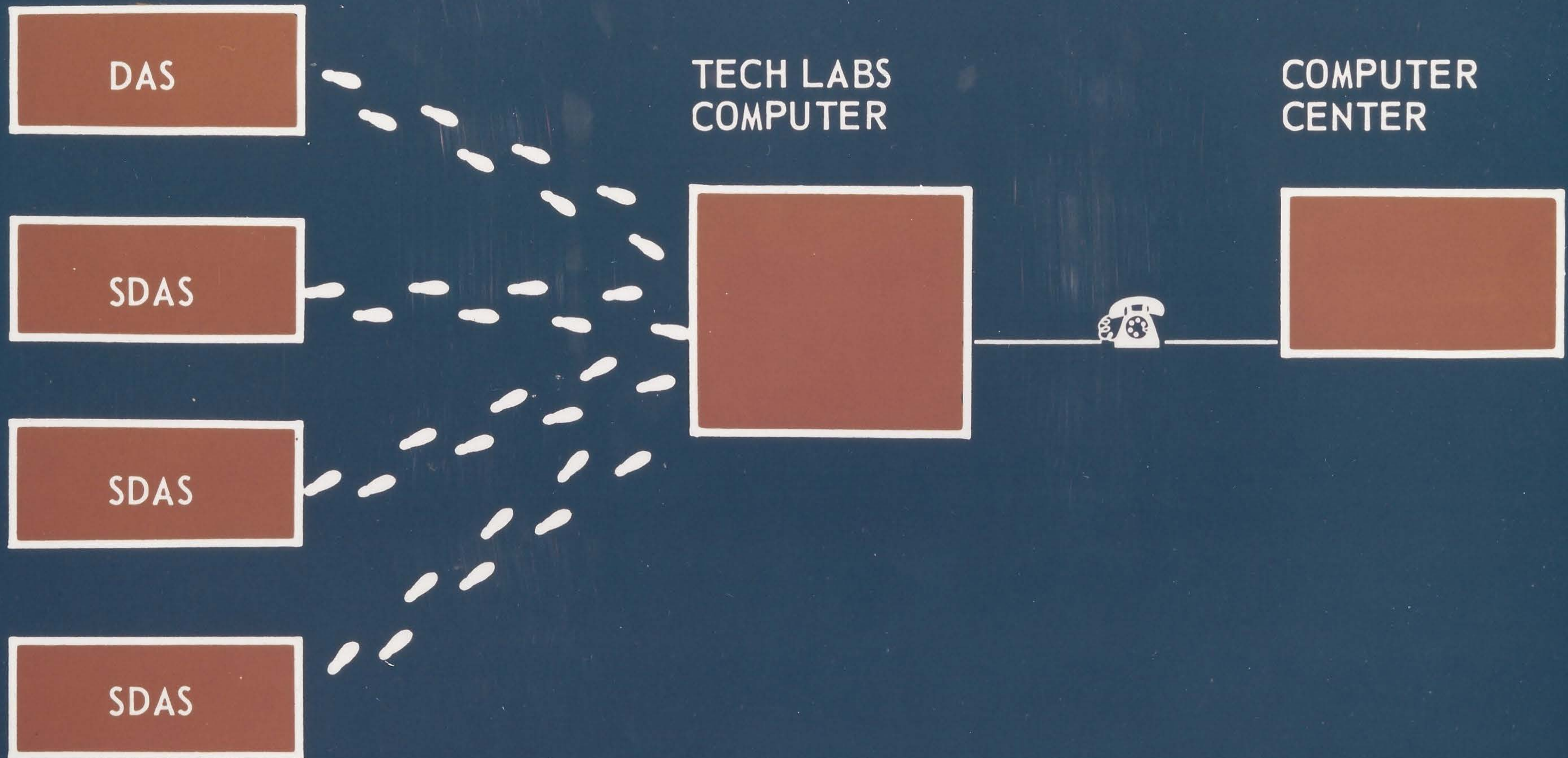
Conclusions and Recommendations

- **CENTRALIZATION VS DECENTRALIZATION**
- **SINGLE VS MULTIPLE STANDARDS**
- **RECORDING MEDIUM**
- **LONG RANGE PLANS**

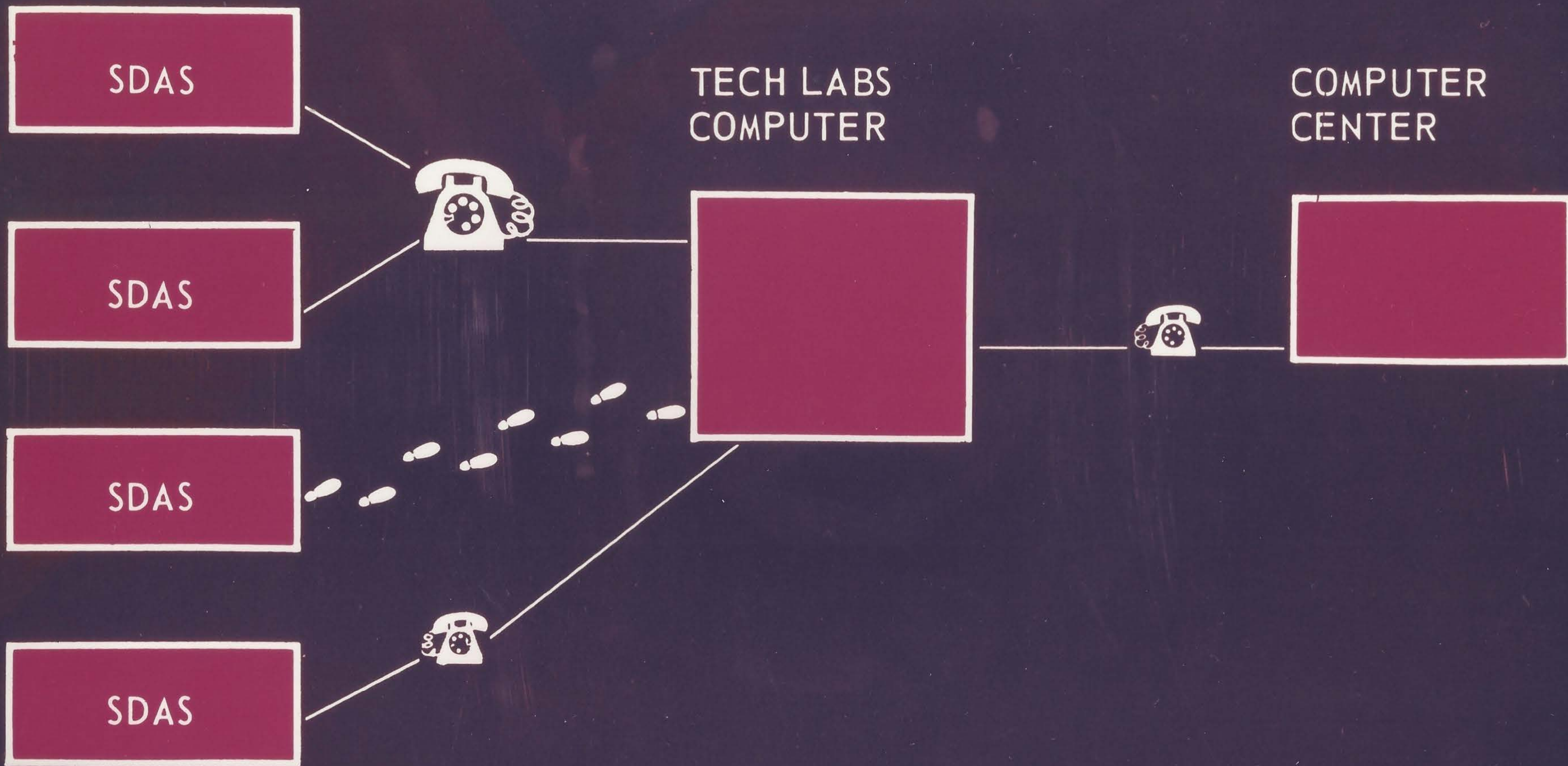
Phase I



Phase II



Phase III



STANDARD DIGITAL DATA ACQUISITION SYSTEM

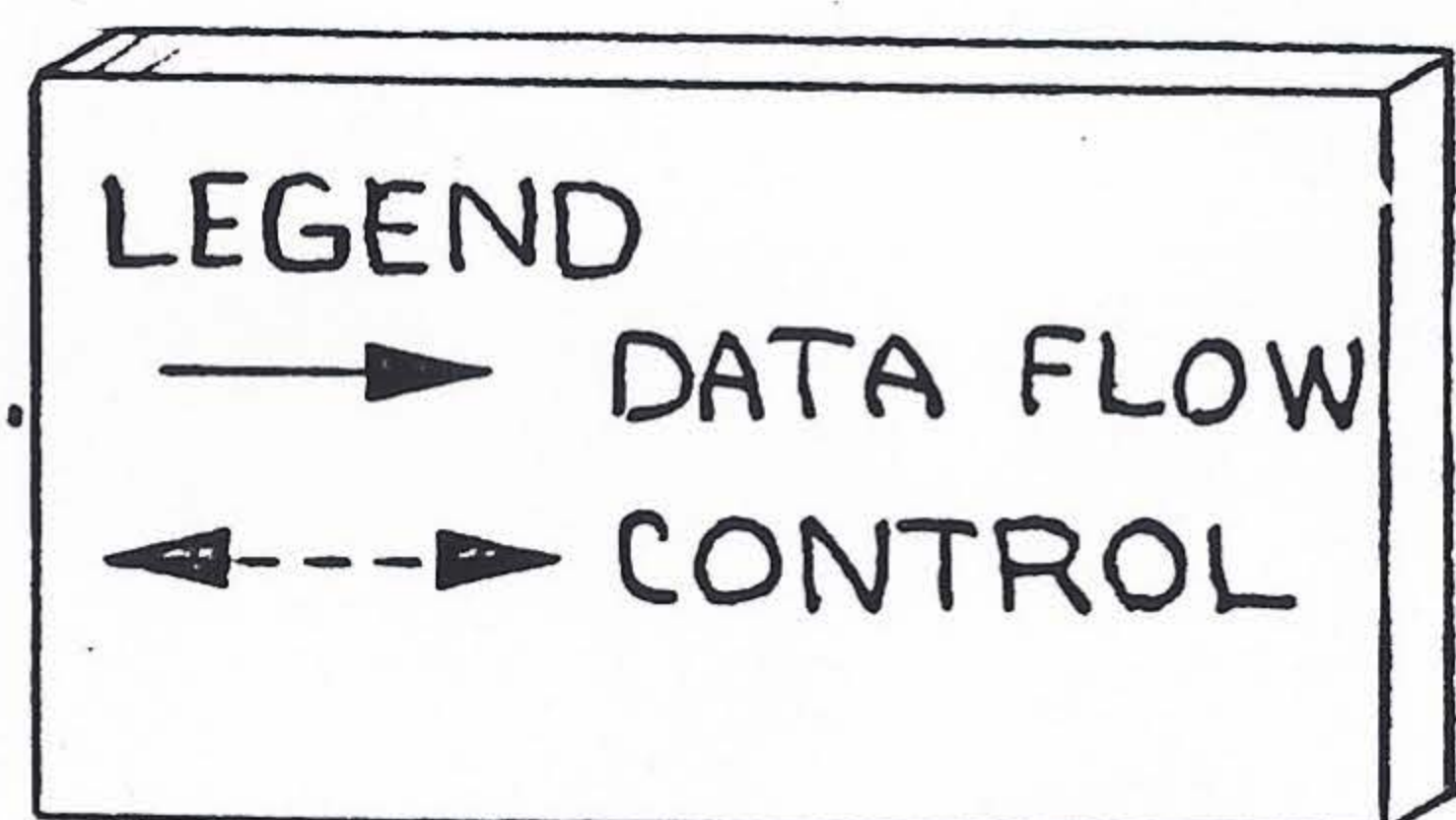
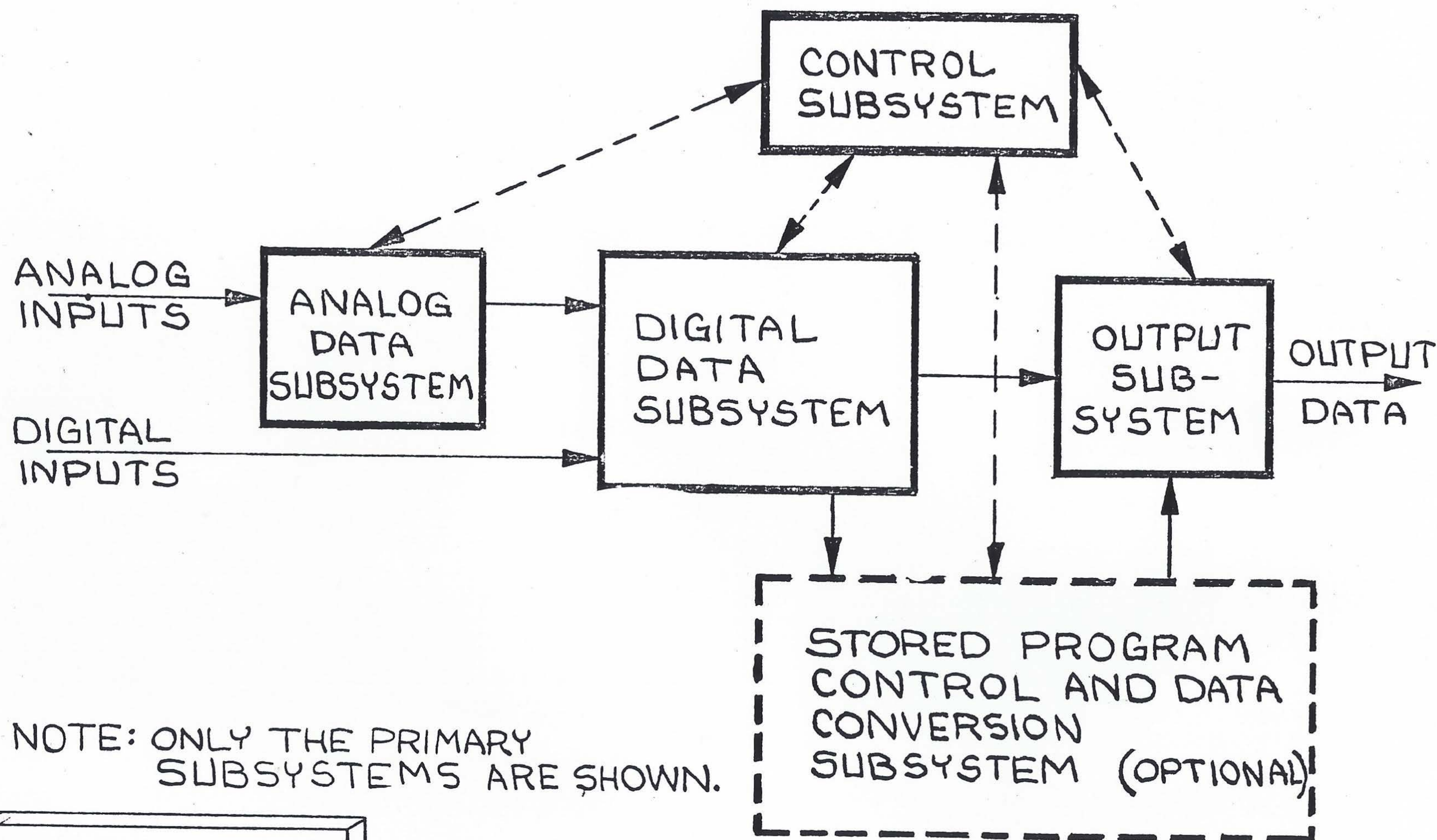


FIG. 3.1.2-1

CALIBRATION
DIRECTOR

RELAY SCANNER
UPPER LIMIT

RELAY SCANNER
UPPER LIMIT

DUAL CROSSBAR
LIMITS
LOWER UPPER

PRESSURE SCAN INTERFACE
UPPER LIMIT DELAY ERROR

PRESSURE
SCANNER

RELAY-SCANNER

HIGH-SPEED SCANNER
0 1 2 3 4 5 6 7 8 9
G G G G G G G G G
A A A A A A A A A

HIGH-SPEED SCANNER
0 1 2 3 4 5 6 7 8 9
G G G G G G G G G
A A A A A A A A A

ANALOG EXPANDER
0 1 2 3 4 5 6 7 8 9

ANALOG BUS

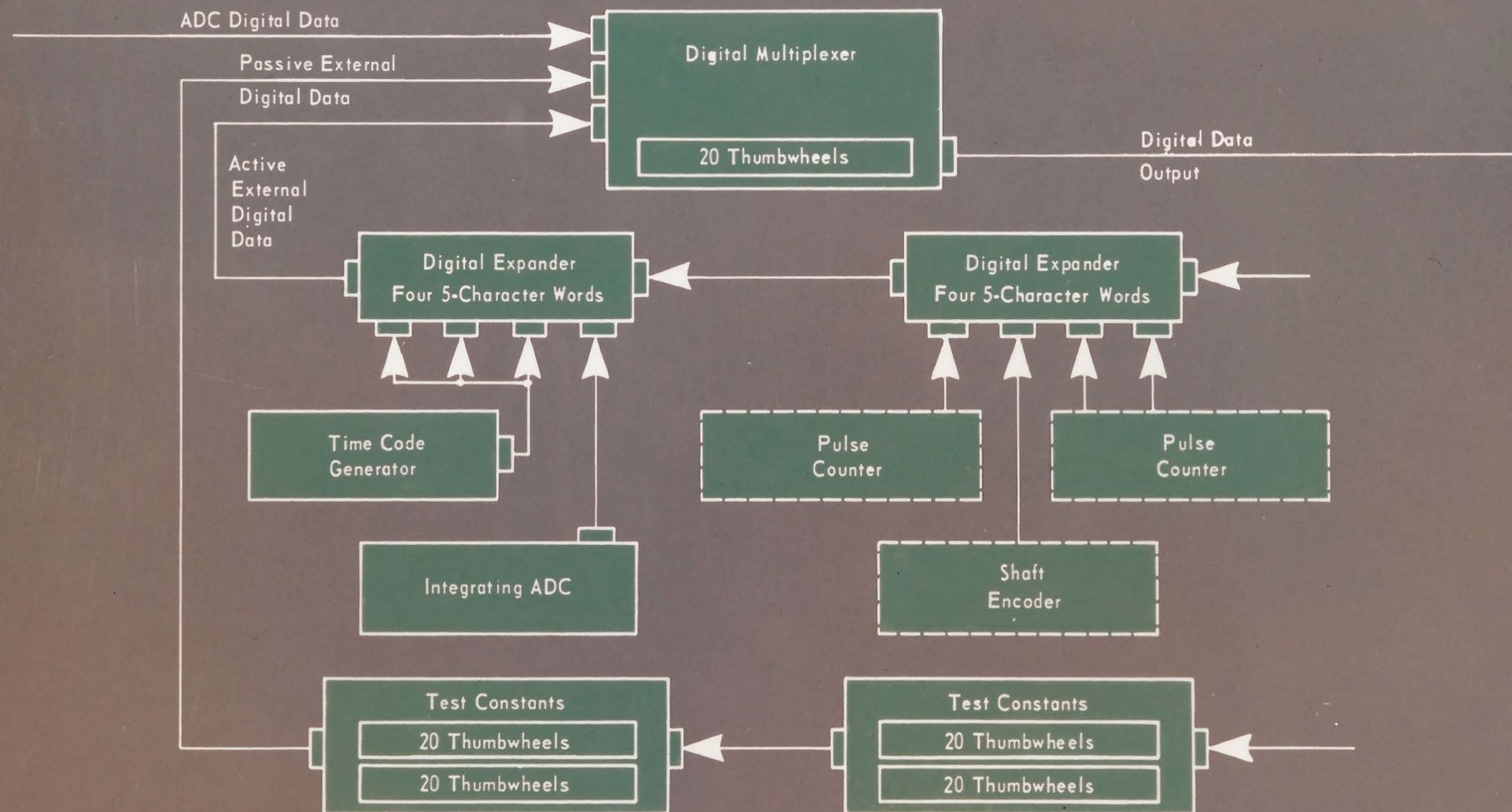
HIGH SPEED ADC
+ 2 3 4 5

OR
INTEGRATING ADC
+ 2 3 4 5

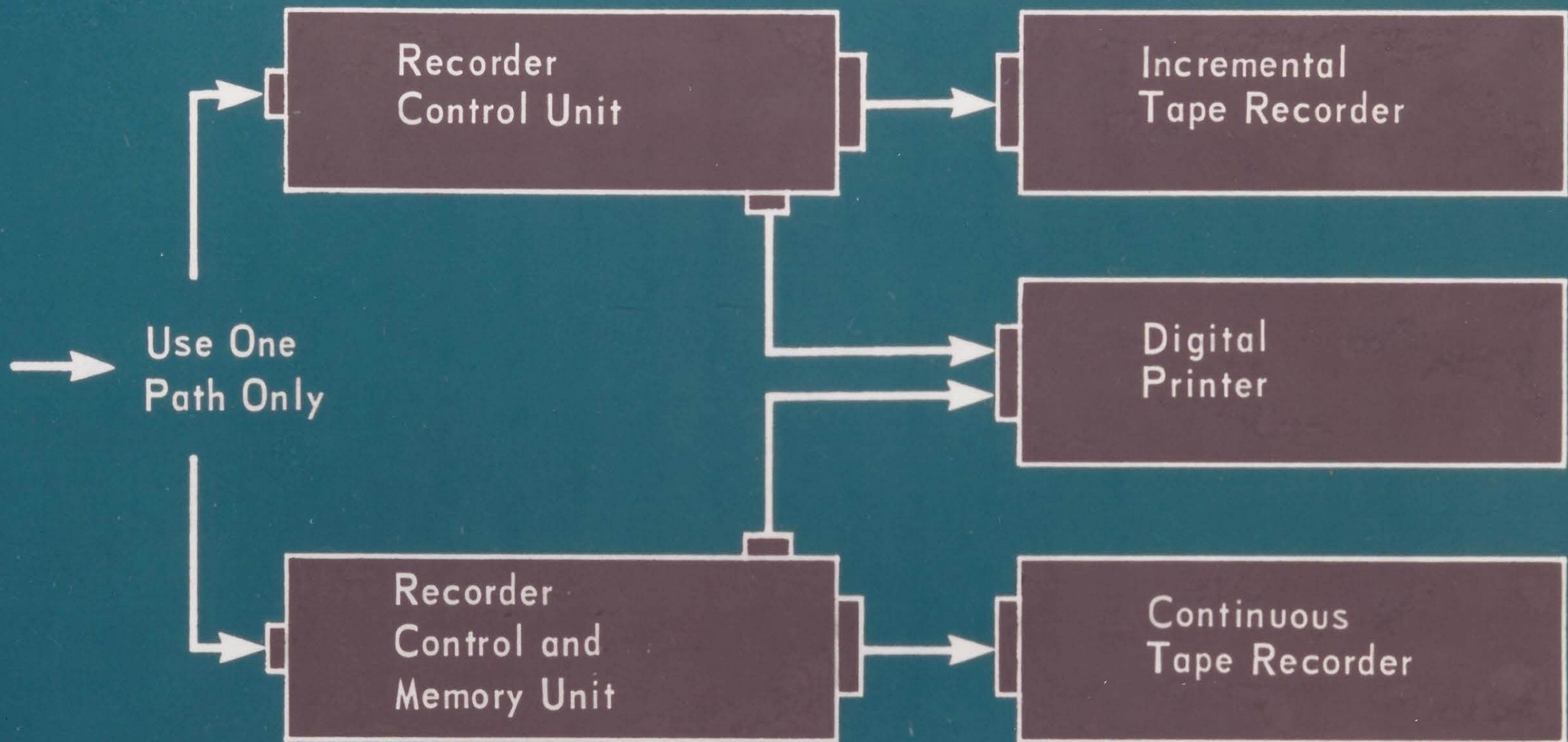
USE
ONE
ONLY

Analog
Data
Sub-
system

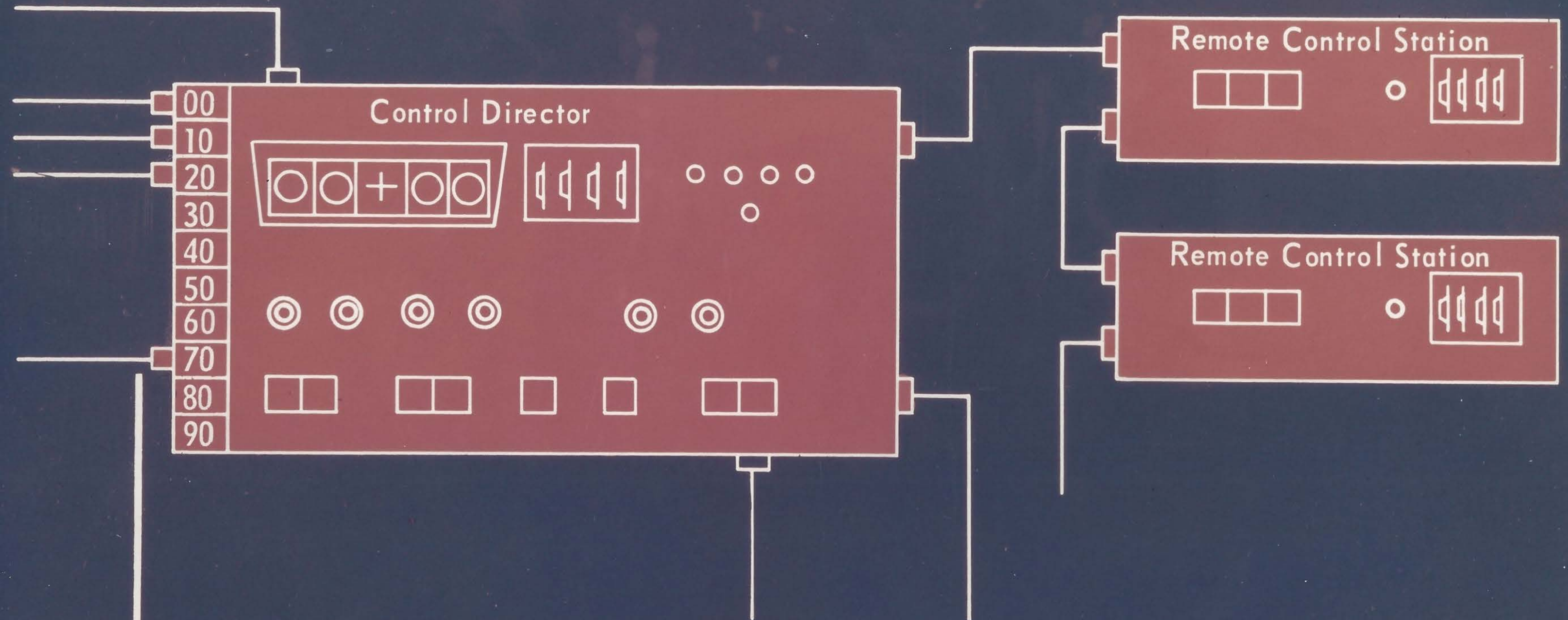
Digital Data Subsystem



Output Subsystem



Control Subsystem



Stored Program Control and Data Conversion Subsystem

